plotted $R_{on,\,spec}$ as a function of N for different values of R_B and R_{Link}. These values are not independent of each other, because they are based on the same diffusion step. We get an increase of $R_{on,\,spec}$ for increasing R_B and R_{Link}. The minimum shifts toward smaller values of N, because R_n approaches its constant value slower than in Fig. 7. In the hypothetic case of a structure without the buried n^+ layer, we would not get a minimum or in other words the minimal specific on-resistance is obtained for one cell, but our model can not be used in this case, because numerical simulations show that the current flow can not be assumed to be vertical under the gate region. In addition, we get a very uniform current distribution under the RESURF area and upwards toward the drain contact.

V. Discussion

The model we have presented can be improved by using analytical expressions for the different resistive elements, which we have extracted from numerical simulations. The difficulty is to get accurate models for the channel and JFET regions. The resistance of the JFET region depends on the gate length and the applied voltage. Several attempts have been made to model this region [6]–[8], but none of them manage without a number of simplifications or approximations. An increase of the gate length would, on the one hand, lead to a decreased JFET resistance, and on the other hand, to a faster increasing total length of the structure. This means, that we are facing a trade-off here. Our model shows that it is better to connect several transistors in parallel than using one huge device, if very large currents should be controlled.

However, it should be repeated here, that the results in this paper are valid for the 2-D case. Consequently, the model could be used when the transistor cells consist of long gate fingers. For the 3-D case, when the gate fingers are laid out in a mesh structure, the model should also provide a fairly good approximation. However, the difficulties mentioned above in determining the R_D are probably more severe in the 3-D case.

VI. Conclusion

This paper has presented an analysis of the specific on-resistance of vertical high-voltage DMOS transistors on SOI substrates. An analytical model has been developed, which accurately predicts the specific on-resistance and its dependency on the number of cells. The model predicts an optimum number of cells, which results in the minimum specific on-resistance. The model shows very good agreement with results from 2-D numerical device simulations.

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An Organic Poly(3,4-Ethylenedioxythiophene) Field-Effect Transistor Fabricated by Spin Coating and Reactive Ion Etching

Tianhong Cui, Guirong Liang, and Kody Varahramyan

***Abstract*—Organic field-effect transistors (OFETs) have been fabricated by the simple and low-cost fabrication processes of spin coating and reactive ion etching (RIE) with poly(styrenesulfonate) doped poly(3,4-ethylenedioxythiophene) as the p-type semiconductor, poly(4-Vinylphenol) as the gate dielectric layer, and polypyrrole (PPy) as the electrodes of gate, source, and drain. The dielectric, semiconductor, gate, and source/drain layers are deposited by low-cost spin coating and patterned with the RIE technique using aluminum thin film as the mask. The electrical characteristics of the device and the influence of PPy on the device performance have been investigated by comparing two types of OFETs with different gates, PPy as one gate and low-resistivity silicon as the other gate in an ambient atmosphere at room temperature. The OFET with PPy as the gate has a field-effect mobility of 0.58×10^{-4} cm^2/V·s with threshold voltage of -13.3 V and subthreshold slope of 6.77 V/decade.**

***Index Terms*—Organic field-effect transistor (OFET), poly(3,4-ethylenedioxythiophene), polypyrrole, reactive ion etching (RIE), spin coating.**

I. Introduction

Due to their low cost, flexibility, and easy processability, organic field-effect transistors (OFETs) have been the focus of enormous technological and scientific efforts for the applications to large-area displays and low-end electronic devices like smart cards. Many attempts in the OFETs have been successfully demonstrated with undoped or doped conjugated polymers such as polyaniline [1], polythiophene [2], poly-3-hexyl-thiophene [3], arylamino-poly-(phenylene-vinylene) [4], and alpha-sexithiophene [5] as the active materials.

To benefit from the various advantages of organic microelectronic devices, there are still several challenges to meet, such as low-cost and batch fabrication processes, novel organic materials with higher conductivities and higher field-effect mobilities, and organic devices comprised of all-organic materials. In this paper, the simple and low-cost procedures to fabricate an OFET as well as its electrical characteristics with poly(styrenesulfonate) doped poly(3,4-ethylenedioxythiophene)

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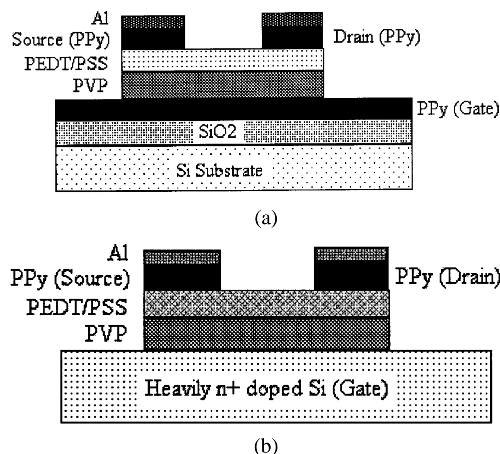

Fig. 1. Schematic cross-sectional view of the organic FETs with PEDT/PSS as the semiconductor.

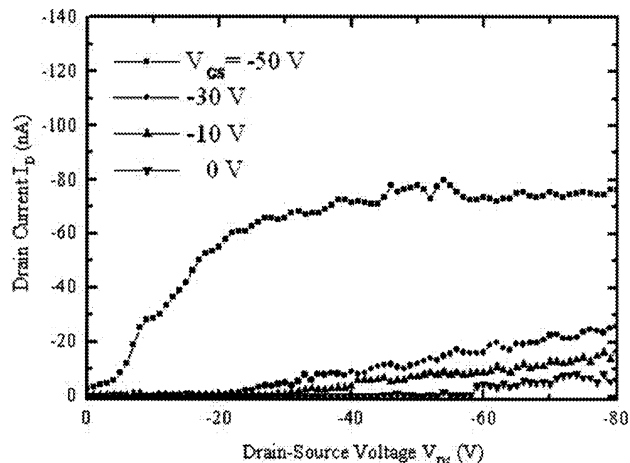

Fig. 2. $\boldsymbol{I_D}$ versus $\boldsymbol{V_{\rm DS}}$ of the organic FET using PEDT/PSS as the semiconductor and PPy as the gate, with a channel length of 40 μm and a channel width of 300 μm.

(PEDT/PSS) as the active layer formed by the low-cost spin coating technique are presented. The simple fabrication processes are comprised of only four spin coatings and two reactive ion etching (RIE) steps with evaporated aluminum as the dry etching mask. In addition, the effect of polypyrrole (PPy) as the gate material on the device performance has also been investigated.

II. Experiments

PEDT/PSS used in our work is a promising p-type semiconductive polymer for electronic applications due to its excellent electrical and optical properties, such as the solution processability, the stability, and the transparent property with light and dark blue color after it is dried [6].

The schematic cross-sectional view of a fabricated OFET with PPy as the gate is shown in Fig. 1(a). For the fabrication of PEDT/PSS OFETs, a silicon wafer coated with 0.5-μm thermal silicon dioxide was used as the substrate. After the wafer was cleaned, the polypyrrole layer about 1 μm thick was spin-coated as the gate electrode and dried on the hot plate. Next, the poly(4-Vinylphenol) (PVP) film 800 nm thick was also spun as the gate dielectric layer. The wafer was cured on the hot plate at 110 $^\circ$C for 5 min to remove all the solvent in the thin film. After baking PVP, the semiconductive polymer PEDT/PSS and the conductive polymer polypyrrole as source/drain electrodes were deposited by spin-coating in sequence. The sample was cured at 115 $^\circ$C for 5 min after each spin-coating step. The thickness of the PEDT/PSS layer and the top PPy layer were 1 μm and 500 nm, respectively. In our work, two reactive ion etching steps were utilized to pattern the polymer layers, and thus formed the device's structures, as shown in Fig. 1(a). Here, a layer of aluminum 120 nm thick was thermally evaporated as the dry etching mask for the RIE process. The first wet etching of aluminum formed the RIE metal mask covering the source, drain, and channel regions. The following RIE etching was used to pattern the top PPy layer and the PEDT/PSS layer. The second wet etching of aluminum formed the source and drain mask for the second RIE etching of the top PPy layer in the channel region and the outside PVP layer. Due to the higher RIE etching rate of PVP than PPy, the PVP in the outside region was etched away before the PPy in the channel region was completely etched. With some reduction in the thickness of the bottom PPy layer, the final device's structures were formed when the top PPy layer in the channel region was completely removed. The electrical characteristics of the fabricated OFET were measured with Keithley SMU236 and 237 measurement units in an ambient atmosphere at room temperature.

III. Results and Discussions

The I_D–$V_{\rm DS}$ drain characteristics of a typical OFET fabricated with PEDT/PSS as the semiconductor and PPy as the source, drain, and gate materials are shown in Fig. 2. This device has a channel length and width of 40 and 300 μm, respectively, and a gate dielectric layer 800 nm thick. In the PEDT/PSS OFETs, the drain current I_D is controlled by the gate voltage $V_{\rm GS}$ applied to the PPy gate. The negative gate voltages will enlarge the conduction channel due to the formation of hole accumulation.

Fig. 2 shows that I_D increases linearly with $V_{\rm DS}$ when $V_{\rm GS}$ is small. When $V_{\rm GS}$ increases to be more negative, I_D rises more steeply at the small drain-source voltages $V_{\rm DS}$ and shows a tendency to saturate at relatively high $V_{\rm DS}$. The characteristics of the OFET show two working regions: linear region and saturation region. Fig. 2 indicates that the PEDT/PSS works as a p-type semiconductor with holes as the majority carriers. When a negative bias is applied to the gate electrode, the holes are attracted to the region between the drain and the source. Under this condition, the conductivity of the channel between the drain and the source is increased with a negative gate bias. Thus, the field effect of this OFET is due to the hole accumulation in the PEDT/PSS layer between the drain and the source.

To analyze the electrical characteristics of the OFET, we assume that the theory for the traditional MOSFET is still effective. In the conventional FET, the drain current in the linear region and the saturation region can be expressed as [7]

$$I_D = \frac{W\mu_{\rm FET}C_i}{L}V_{\rm DS}(V_{\rm GS}-V_{\rm th}) \quad (1)$$

$$I_{\rm Dsat} = \frac{W\mu_{\rm FET}C_i}{2L}(V_{\rm GS}-V_{\rm th})^2 \quad (2)$$

where W and L are the channel width and length, respectively, $\mu_{\rm FET}$ is the carrier mobility of the holes in the PEDT/PSS channel, $C_i = \varepsilon_i/d_i$ is the gate dielectric capacitance per unit area (ε_i and d_i are the dielectric constant and the film thickness of the gate dielectric layer, respectively), and $V_{\rm GS}$, $V_{\rm DS}$, $V_{\rm th}$ are the gate voltage, the drain-source voltage, and the threshold voltage, respectively.

Fig. 3 shows the measured gate transfer characteristics of the PEDT/PSS OFET with PPy as the gate. By linearly extrapolating the curve to the $V_{\rm GS}$ axis, the threshold voltage $V_{\rm th}$ can be extracted to be -13.3 V. It indicates that the OFET is a normally off transistor.

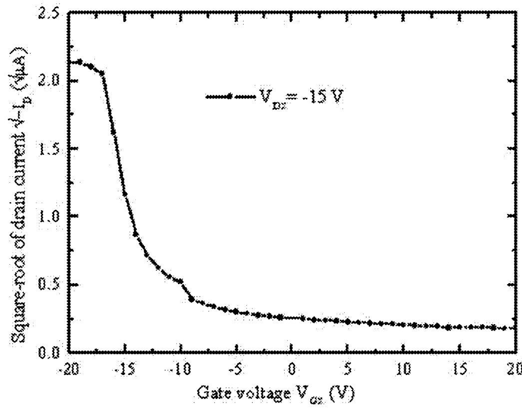

Fig. 3. Gate transfer characteristics of the organic FETs using PEDT/PSS as the semiconductor and PPy as the gate, with a channel length of 40 μm and a channel width of 300 μm.

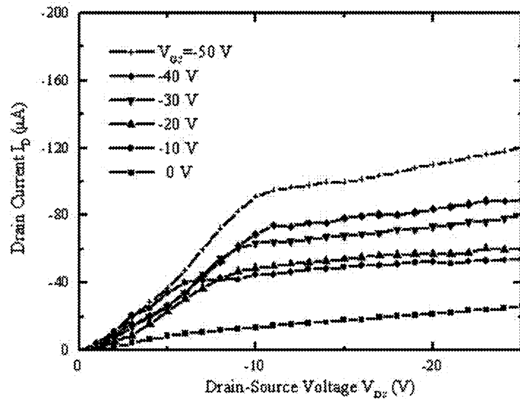

Fig. 4. Drain characteristics of the PEDT/PSS OFET using a heavily n^+ doped silicon as the gate and the substrate, with a channel length of 40 μm and channel width of 300 μm.

The hole mobility $\mu_{\rm FET}$ in the linear region with a small $V_{\rm DS}$ of -15 V can be extracted to be 0.58 $\times$ 10^{-4} cm^2/V·s from Fig. 3. When the $V_{\rm DS}$ of -15 V was applied and the gate voltages were swept from 20 to -20 V, the subthreshold slope was obtained to be about 6.77 V/decade.

For the influence of different gate materials on the performance of the OFETs, an OFET with similar structures, shown in Fig. 1(b), has also been fabricated in a similar approach, except that the gate material (PPy) was replaced by a heavily n^+ doped silicon wafer (resistivity of 0.01 Ω·cm). Fig. 4 shows the drain characteristics of this PEDT/PSS OFET with a channel length and channel width of 40 and 300 μm, respectively. Based on the analysis method stated above, the main extracted electrical parameters of this OFET are field-effect mobility of 0.8 cm^2/V·S, threshold voltage of 9.3 V, and subthreshold slope of 4.5 V/decade.

By comparing the electrical characteristics of the above two OFETs with the same channel length and width under the same bias voltages, the PEDT/PSS OFET with PPy as the gate has a drain current near thousand times smaller, much lower field-effect mobility, higher threshold voltage, and larger subthreshold slope than the OFET with heavily doped silicon as the gate. The main differences observed between the two OFETs should be attributed to the electrical properties of the gate material PPy and the dielectric material PVP. First, the different work functions of PPy and n^+ doped silicon will cause the work function difference between the gate and the semiconductor, and thus result in different energy band bending. Second, there is a leakage current, on the order of 10^{-10} A, flowing through the dielectric layer (PVP) during the measurement. When this gate leakage current flows through the gate series resistance formed by the gate material PPy, the reduction of effective gate voltage applied on the gate insulator $\Delta V_{\rm GS}$ is proportional to the resistivity and the gate leakage current according to the following:

$$\Delta V_{\rm GS} = V_{\rm GS} - V_{\rm GSeff} = R_G I_{\rm GS} = \frac{L}{A}\,\rho I_{\rm GS} \tag{3}$$

where $V_{\rm GSeff}$ is the effective gate voltage, R_G is the gate series resistance, $I_{\rm GS}$ is the gate leakage current, ρ is the resistivity of PPy material, and L and A are the thickness and the effective area of the gate electrode, respectively.

Thus, the effective electrical field of the applied gate voltage is decreased about 100 times due to the smaller conductivity of PPy (generally less than 1 S/cm), compared to that of n^+ doped Si, and much fewer carriers will be attracted to form the conduction channel between the drain and the source. It means that a much larger gate voltage $V_{\rm GS}$ applied on the OFET with PPy as the gate is necessary to achieve the drain current in the same order due to the largely weakened field effect. The larger subthreshold slope indicates that the device speed of the OFET with PPy as the gate is lower.

For practical applications, the OFETs are required to have smaller threshold voltages. Therefore, PPy as the gate material strongly affects the electrical characteristics of the OFET. To improve the performance and benefit from the various advantages of the OFETs, we need to investigate the conductive polymers with higher conductivities to work as the electrodes (the gate, the source, and the drain) and other solution processable dielectric materials to reduce the leakage currents. These will be the focus of further research on polymer microelectronic devices.

IV. Conclusion

In summary, based on the simple and low-cost fabrication processes including spin coating and RIE with aluminum as the dry etching mask, the OFETs with PEDT/PSS as the semiconductor have been successfully fabricated, and their electrical characteristics have been investigated in an ambient atmosphere at room temperature. All-organic materials were deposited by spin coating and patterned by RIE dry etching. This simple and low-cost fabrication technique may pave the way to fabricate all-organic FETs and circuits with other organic or polymer materials for practical applications. The influence of PPy as the gate material on the device characteristics has also been studied. Further research to improve the properties of the OFETs may focus on the organic semiconductors with higher carrier field-effect mobility, organic dielectrics with better quality, and conductive polymers with higher conductivity as the electrodes.

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Fast Reverse Recovery Body Diode in High-Voltage VDMOSFET Using Cell-Distributed Schottky Contacts

Xu Cheng, Johnny K. O. Sin, Baowei Kang, Chuguang Feng, Yu Wu, and Xingming Liu

***Abstract*—A new approach to improve the high-voltage vertical double-diffused MOSFET (VDMOSFET) body-diode recovery speed is proposed. In this approach, a Schottky contact is integrated into every cell of the VDMOSFET. Experimental results from the fabricated samples show a 50% decrease in the reverse recovery charge and a 60% increase in the softness factor of the body diode in 500 V/2 A VDMOSFETs.**

***Index Terms*—Body diode, recovery speed, Schottky contact, VDMOSFET.**

I. Introduction

Conventionally, a vertical double-diffused MOSFET (VDMOSFET) structure contains a parasitic body diode formed by the p-well and the n^--drift region. In bridge topologies for applications such as motor control, this internal diode is very advantageous to be used as a freewheeling diode. However, its slow reverse recovery results in a significant increase in the switching power losses and seriously limits its usages. Several methods have been reported to improve the reverse recovery speed of the body diode. In the low-voltage range (breakdown voltage lower than 50 V), it was suggested to integrate a lumped Schottky diode in the center of the VDMOSFET chip [1], [2] to bypass the parasitic body diode. However, this approach cannot be used in a high-voltage device due to the poor blocking capability of the lumped Schottky diode. In the high voltage range (breakdown voltage higher than 200 V), usually carrier-lifetime-control techniques are employed. Irradiation by electron [3] or by proton [4] have been demonstrated to be effective in reducing the reverse recovery charge $(Q_{\rm rr})$ of the body diode; however, the VDMOSFET characteristics, such as the threshold voltage, leakage current, and breakdown voltage, are significantly sacrificed due to the damage induced by irradiations [3]–[5]. These parameters are liable to age easily. The finely controlled platinum implantation and diffusion is very effective to reduce the $Q_{\rm rr}$ [6]; however, this technique requires some sophisticated processes which involve heavy metals that are generally contaminative to the fabrication process.

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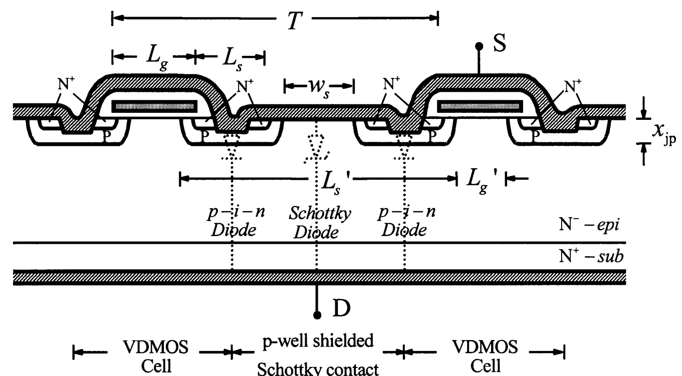

Fig. 1. Schematic cross section of Schottky integrated high-voltage VDMOSFET structure. Notes: $\boldsymbol{L}_g$ is the width of the poly-si gate on the mask; $\boldsymbol{L}_s$ is the width of the p well on the mask; $\boldsymbol{x}_{\rm jp}$ is the p-well junction depth; $\boldsymbol{L}_g'$ is the spacing between the p wells under a poly-Si gate; $\boldsymbol{w}_s$ is the realized Schottky contact width; $\boldsymbol{L}_s'$ is the equivalent p-well width; and $\boldsymbol{T}$ is the width of the periodic cell.

In this paper, a new cell-distributed Schottky-contact structure is developed for the high-voltage VDMOSFET's application to improve the body-diode recovery speed. This approach has the advantages of no contamination, no aging of the electrical parameters, unaffected threshold voltage, and very easy implementation. Experimental results from the fabricated VDMOSFET samples with different Schottky-contact size in the cells are presented. Meanwhile, the simulations are carried out by using MEDICI[1] to exploit the case of different process linewidth.

II. VDMOSFET Structure With Cell-Distributed Schottky Contacts

Although the trench-gate structure is widely adopted as the modern low-voltage power MOSFET technology, the planar-gate structure still prevails in the high-voltage power MOSFET fabrication for its high ruggedness, technological simplicity, and the trifle influence of the "JFET" resistance in on-resistance of the high-voltage MOSFET. Based on the conventional high-voltage VDMOSFET structure, a new structure is proposed to improve the body-diode speed. Fig. 1 shows the schematic of the new VDMOSFET structure equipped with cell-distributed Schottky contacts. Fig. 1 also defines the various dimensions of the structure. In the structure, the Schottky contact is integrated into every cell of the VDMOSFET. The body diode is then composed by pn junctions and paralleled Schottky contacts. When this composed body diode is turned on, a part of the current will flow through the Schottky contacts in the form of majority carrier current. So, the injected minority carriers, and then the stored excess carriers, in the n^--drift region are reduced during the on-state, which enables a fast recovery when the body diode is turned off. On the other hand, the blocking capability of the Schottky contact is improved with this cell-distributed structure [7]. When a high voltage is applied at the drain electrode, the Schottky contacts will be electrostatically protected by the adjacent p wells as the depletion layers from the adjacent p wells will pinch off the n^- region under the Schottky contact. Thus, the electric field under the Schottky contact is reduced.

[1]Trademarked.